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16. Abstract

This document presents a development plan for a proposed Avionics Test Bed facility for the early investigation and evaluation of new concepts for the control of Large Space Structures, Orbiter attached flex body experiments, and Orbiter enhancements. This plan outlines a distributed data processing facility that will utilize the current JSC laboratory resources for the test bed development. This document defines the future studies required for implementation, the management system for project control, and the baseline system configuration.

The attached appendix provides a background analysis of the specific hardware system for the preliminary baseline Avionics Test Bed system.

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APPENDIX A

ALGORITHMS FOR VLSI PROCESSOR ARRAYS

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ALGORITHMS FOR VLSI PROCESSOR ARRAYS

It is anticipated that a large flexible space structure will require substantial computational support from onboard data processing elements. The availability of Very Large Scale Integrated (VLSI) circuits offers an alternative to conventional computers and algorithms. Processors and memory elements can be easily implemented in VLSI. Processor arrays and concurrent algorithms can be evaluated in the Avionics Test Bed (ATB).

Mead and Conway in their book "Introduction to VLSI Systems" present several concurrent algorithms for vector and matrix operations. A nondimensional timing factor is used to compare processing time between processor arrays and a uniprocessor. The nondimensional time unit is the amount of time required to compute:

$$R_C = R_C + R_A \times R_B$$

Where R_A, R_B, and R_C are registers. This recurrence relation is the heart of all matrix-vector and matrix-matrix multiplication algorithms and can be performed using the innerproduct processor shown in figure A-1(a).

The basic network organization of array processors is mesh connected where all connections from a processor are to neighboring processors. Linearly and hexagonally connected arrays are natural for matrix problems (figure A-1(b)).

The linearly connected array is applicable to matrix-vector multiplication. The required multiplication is indicated in figure A-2 for a band matrix. The width of a band matrix is $w = p + q - 1$. The linearly connected processor network for this example is shown in figure A-2. The required width of the array is $w = 2 + 3 - 1 = 4$.

The inputs and outputs are pipelined through the processors as indicated in figure A-2. The algorithm and timing are discussed in detail in Mead and Conway. The first seven steps of the pipeline algorithm are presented in figure A-3. For a matrix of bandwidth w, the first complete multiplication is complete after w time units. Then the components of $y = Ax$ start shifting out

from the left end processor at the rate of one output every two units of time. Therefore, using a network of w processors, all n components of y can be computed in 2n + w time units as compared to the order of wn (for large n) time needed for the sequential algorithm on a uniprocessor. Several numerical examples are presented in table A-1. Notice in figure A-2 that only w/2 processors are busy at any one time so it is possible to use one half of the indicated processors. The number of array processors is dependent on w and not on the size of the matrix.

The comparative performance factor indicates the increased performance obtained by an array of processors. An example performance comparison is shown for a 12 × 12 matrix of bandwidth 6. An array of 3 processors will be 2.1 times faster than a comparable uniprocessor.

For a dense matrix, $w = 2n - 1$ is used to compute the array time factor. The uniprocessor time factor is n^2. Several numerical examples for dense matrices are presented in table A-1. A 10 × 10 dense matrix can be multiplied by a vector using an array of 10 processors. The array will be 2.6 times faster than a comparable uniprocessor. Dense matrices require large arrays to obtain a meaningful gain in performance.

The hex-connected processor array can be used for matrix-matrix multiplication. An example band matrix multiplication is presented in figure A-4. The first four steps of the matrix multiplication are exhibited in figure A-5. The required array size is w_1w_2 which is 4 × 4 = 16 for this example. Note that only one-third of the processors are active at any one time so it is possible to use approximately $1/3w_1w_2$ processors.

Some sample performance comparisons are presented in table A-2. The hex-connected array is particularly suited for band matrices. The required number of hex-connected processors is dependent upon the bandwidths and not the dimensions of the matrices. Example (1) in table A-2 demonstrates that an array of 6 processors will be 3.8 times faster than a uniprocessor. Example (2) in table A-2 shows that large arrays are required if the matrices are dense. An array of 41 processors is required to multiply two 6 × 6 matrices. The array would be 7.4 times faster than a uniprocessor.

Processor arrays are suitable for other algorithms such as the LU-Decomposition of a matrix, triangular linear systems, convolution, finite impulse response (FIR) filters, and discrete Fourier transforms. The important feature common to all of the algorithms is that the data flows are simple and regular. Almost all processors needed in the arrays are the inner product step processor to perform $R_C = R_C + R_A \times R_B$. The processing elements are uniform, interprocessor connections are simple and regular, and external connections are minimized. Construction of these arrays should prove to be cost effective. The ATB is a natural resource to test candidate arrays and algorithms that are applicable to large space structures.

TABLE A-1.- MATRIX-VECTOR MULTIPLICATION
LINEAR ARRAY VS UNIPROCESSOR

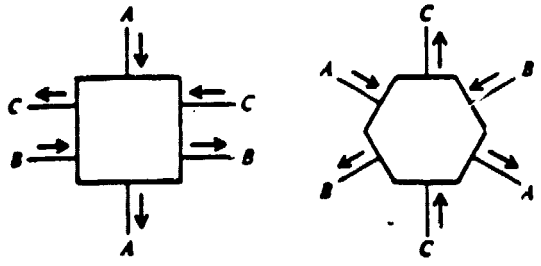
n	p	q	w	Required time		Minimum/ array processors (w/2)	Comparative performance factor*
				array (2n + w)	uniprocessor		
Band Matrix			(p + q - 1)		(actual count)		
6	2	3	4	16	20	2	1.25
10	3	4	6	26	51	3	2.0
12	3	4	6	30	63	3	2.1 (1)
100	3	4	6	206	570	3	2.8
Dense Matrix			(2n - 1)		(n^2)		
10	10	10	19	39	100	10	2.6 (2)
12	12	12	23	47	144	12	3.1

*Uniprocessor time/array time
(1) 63/30 = 2.1 (A 3 processor array improves performance by a factor of 2.1)
(2) 100/39 = 2.6 (A 10 processor array improves performance by a factor of 2.6)

TABLE A-2.- MATRIX-MATRIX MULTIPLICATION
HEX-CONNECTED ARRAY VS UNIPROCESSOR

n	w_1	w_2	Required time		Minimum number of processors $1/3(w_1 w_2)$	Comparative performance factor*
			array $(3n + w)$	uniprocessor		
Band Matrices				(actual count)		
6	4	4	22	71	approx. 6	3.2
10	4	4	34	130	" 6	3.8 (1)
10	6	6	36	262	" 12	7.3
Dense Matrices				(n^3)		
6	11	11	29	216	" 41	7.4 (2)
10	19	19	49	1000	" 121	20.4
12	23	23	59	1728	" 176	29.3

*Uniprocessor time/array time
(1) 130/34 = 3.8 (A 6 processor array improves performance by a factor of 3.8)
(2) 216/29 = 7.4 (A 41 processor array improves performance by a factor of 7.4)



Geometries for the inner product step processor.

Figure A-1(a).- Inner product processor

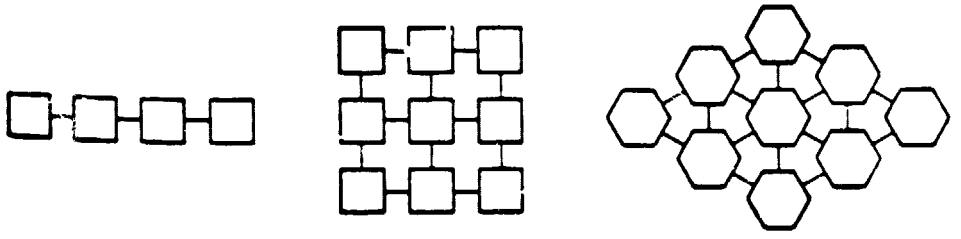
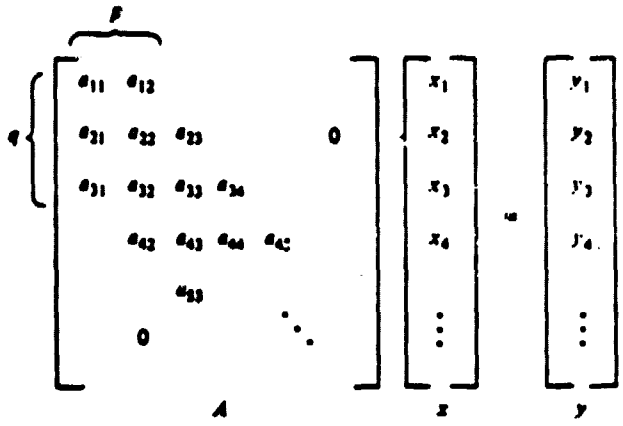
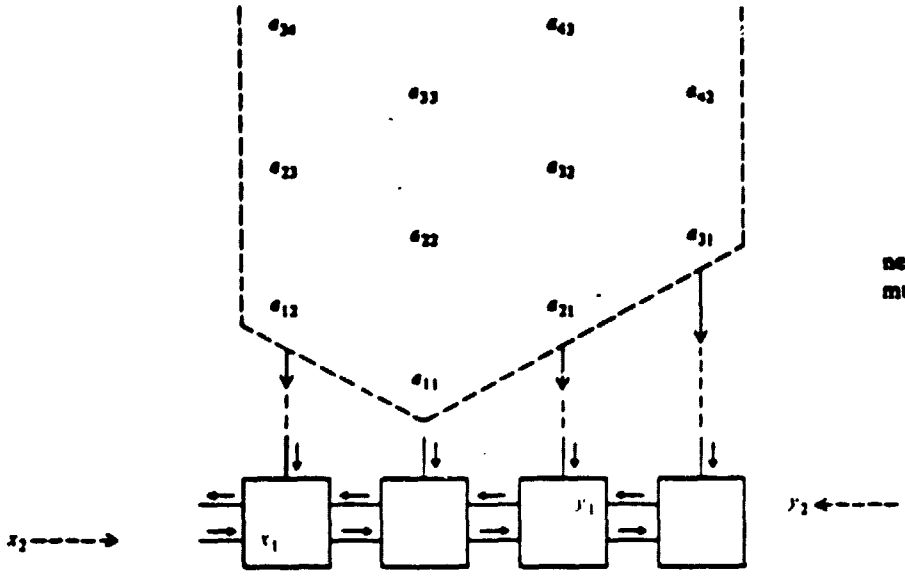


Figure A-1(b).- Mesh connected processor arrays.

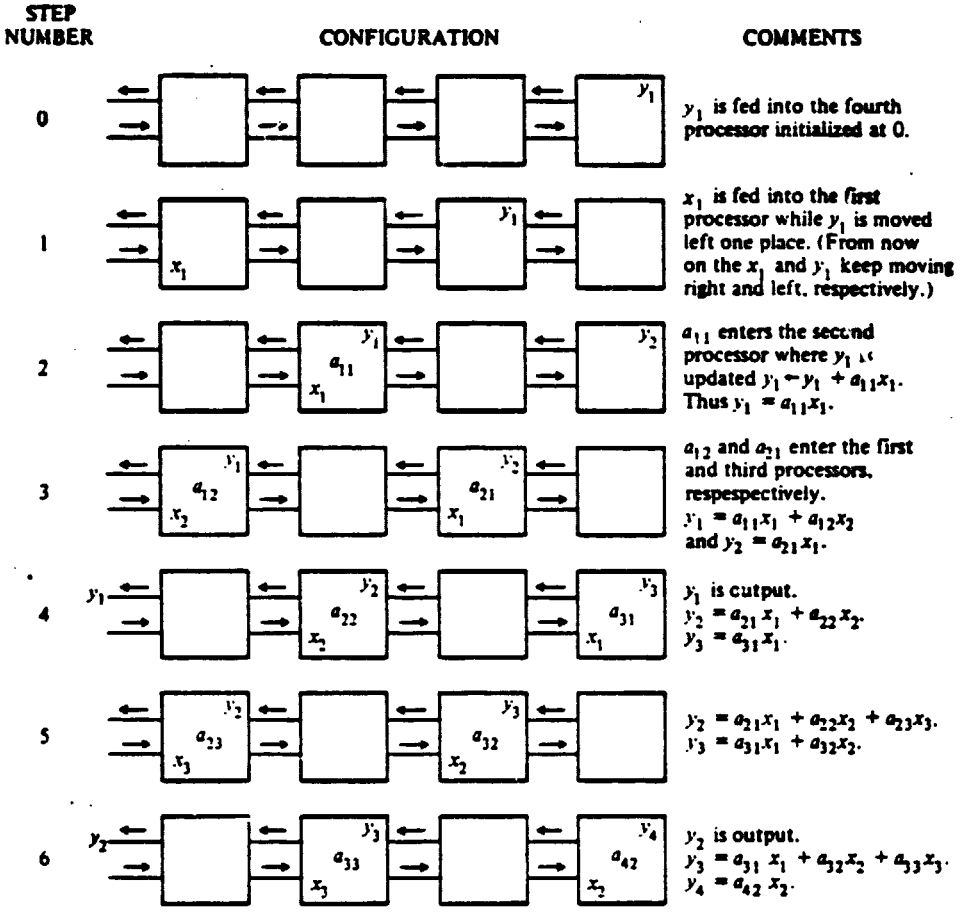


Multiplication of a vector by a band matrix with $p = 2$ and $q = 3$.



The linearly connected network for the matrix–vector multiplication problem

Figure A-2.- An example of an array processor.

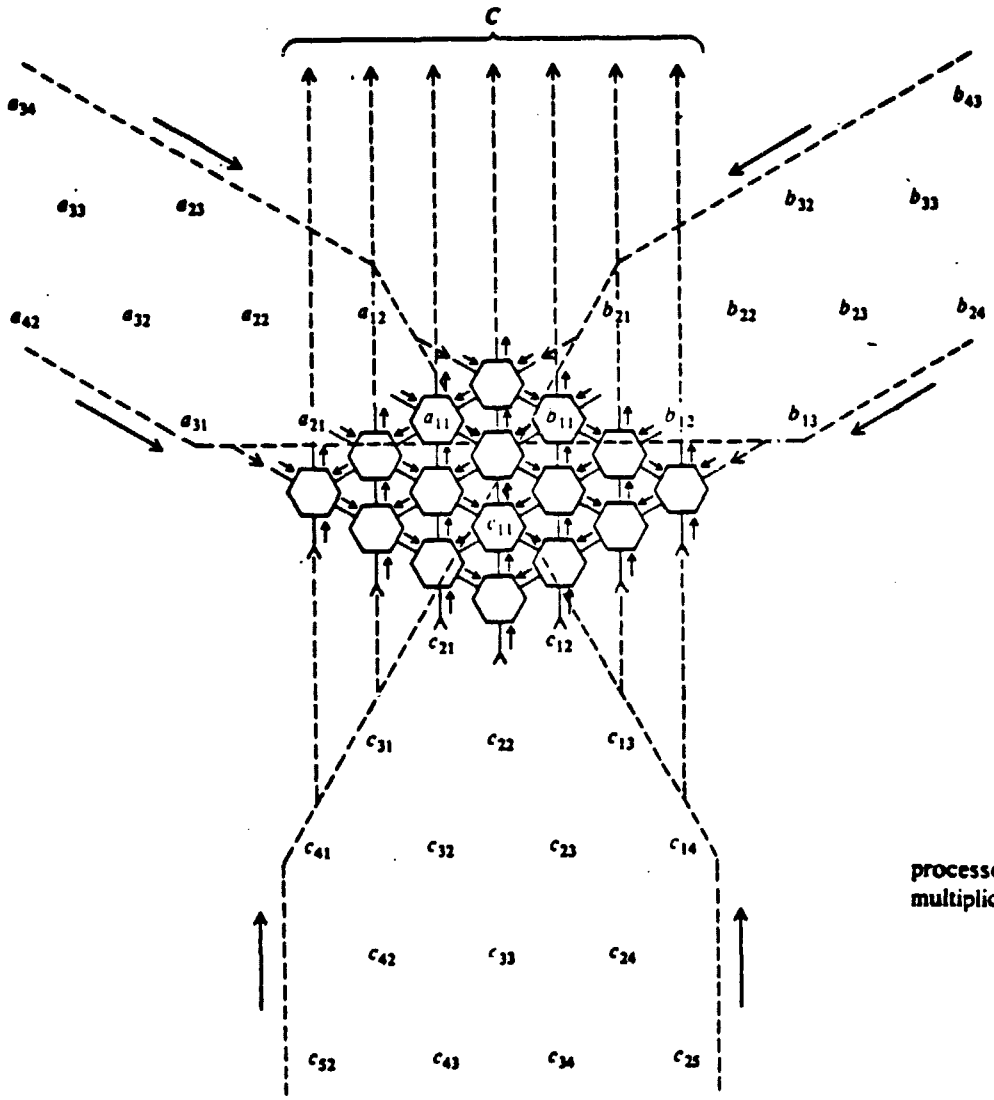


The first seven steps of the matrix-vector multiplication algorithm.

Figure A-3.- An example of a pipeline algorithm.

$$\begin{bmatrix} a_{11} & a_{12} & & & 0 \\ a_{21} & a_{22} & a_{23} & & \\ a_{31} & a_{32} & a_{33} & a_{34} & \\ & a_{42} & \ddots & \ddots & \\ 0 & & & & \end{bmatrix} \quad A \qquad \begin{bmatrix} b_{11} & b_{12} & b_{13} & & 0 \\ b_{21} & b_{22} & b_{23} & b_{24} & \\ & b_{32} & b_{33} & b_{34} & b_{35} \\ & & b_{43} & \ddots & \ddots \\ 0 & & & & \end{bmatrix} \quad B \qquad = \qquad \begin{bmatrix} c_{11} & c_{12} & c_{13} & c_{14} & 0 \\ c_{21} & c_{22} & c_{23} & c_{24} & \\ c_{31} & c_{32} & c_{33} & c_{34} & \\ c_{41} & c_{42} & & \ddots & \\ 0 & & & & \end{bmatrix} \quad C$$

Band matrix multiplication.



The hex-connected processor array for the matrix multiplication problem

Figure A-4.- A hex-connected multiprocessor array.

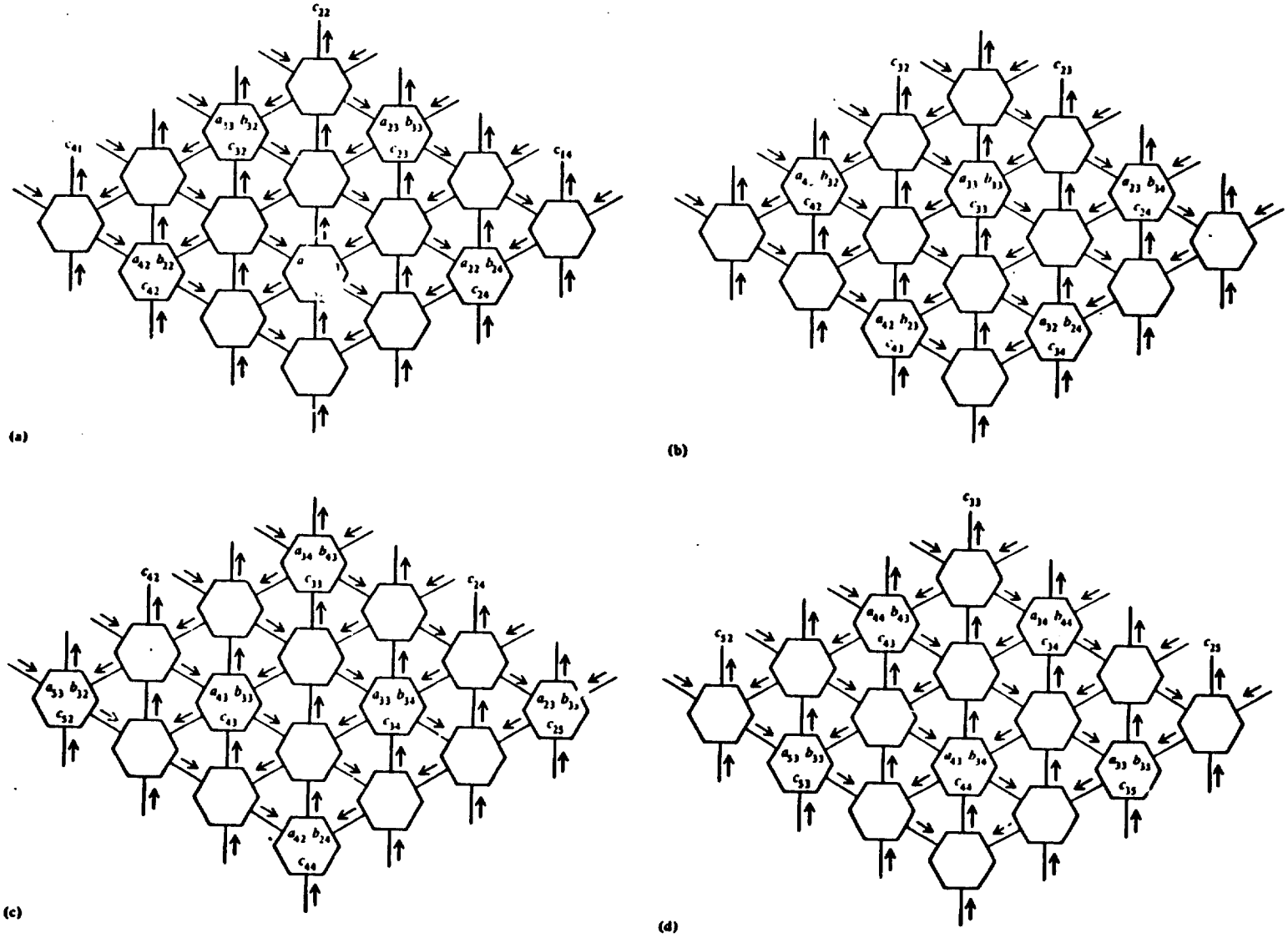


Figure A-5.- Four steps during matrix multiplication shown in Figure A-4.

APPENDIX B

HTS MICROPROCESSOR EVALUATION

APPENDIX B

HTS MICROPROCESSOR EVALUATION

B.1 DATA MANAGEMENT SYSTEMS SOFTWARE BACKGROUND

The DMT shown in figure B-1 programming support environment consists of a Real Time Multitasking Operating System and a High Level Language interface.

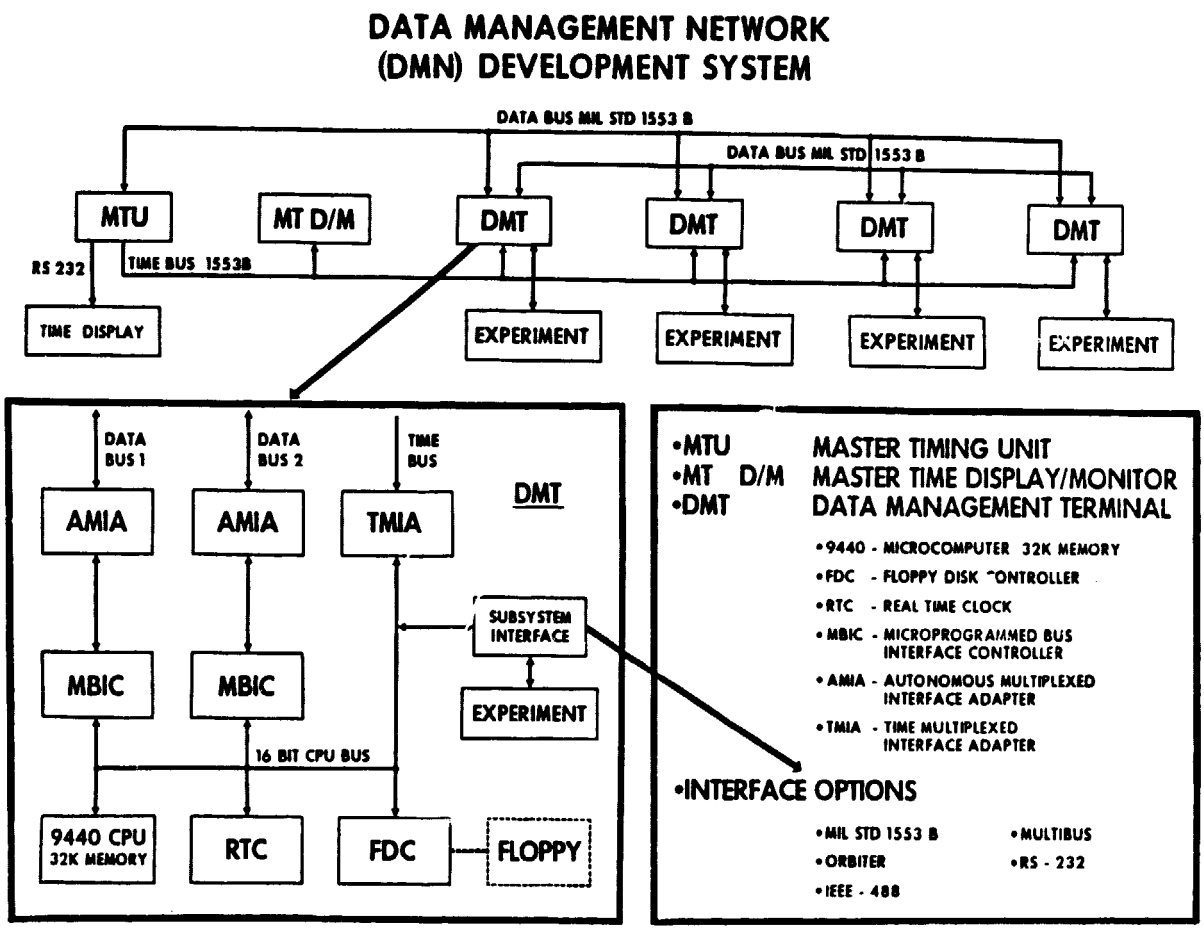


Figure B-1.- Data management development system.

The operating system performs scheduling for event driven software. An event may be the result of an interrupt, the completion of a calculation, or a signal from one task to another. Programs are divided into concurrently executed

task modules. These tasks share the CPU and other resources local to the subsystem. Each task is assigned a priority and the CPU is switched to the highest priority task which is ready to execute. Memory is divided into code and data segments. Memory is statically allocated for code segments and dynamically allocated for data segments. At the beginning of execution, all available space for data is divided equally into segments.

Each active task is assigned a segment for its local variables. (Common blocks are assigned statically.) Figure B-2 shows an approximate layout of the microprocessor's memory.

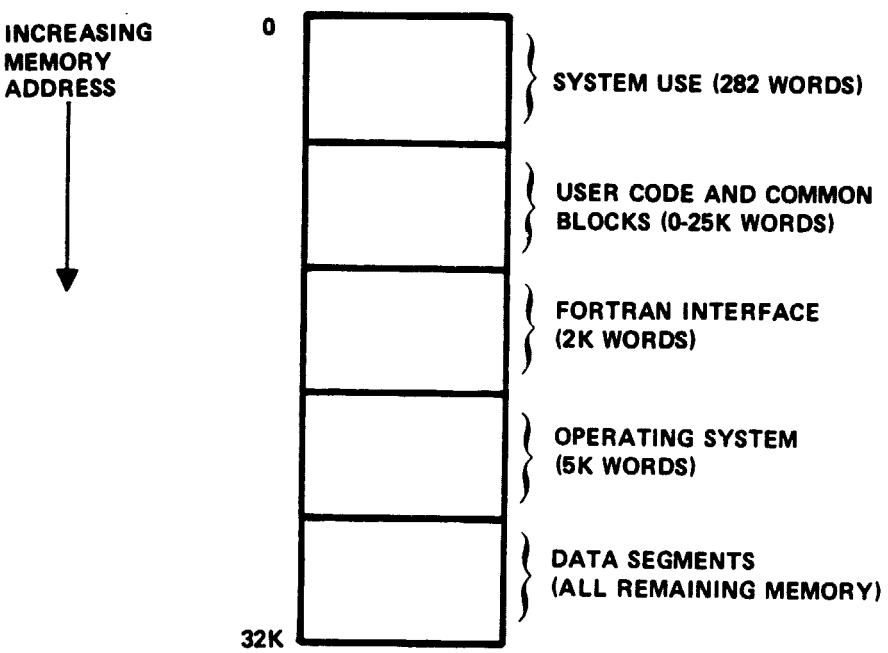


Figure B-2.- HTS processing mode memory map (for minimum system configuration).

The high level language interface consists of a set of FORTRAN callable subroutines to communicate with the operating system's task schedules, the time bus (TMIA), system buses (MBICs), and local peripherals. In particular, a FORTRAN applications program can originate, receive, and time tag internode messages.

For detailed information on the system just described, reference the following documents.

--	9440 Microprocessor Technical Manual
--	Floppy Disk Technical Manual (LEMSCO)
LEMSCO-15674	Dual Floppy Disk Driver User's Guide
JSC-16770	
LEMSCO-15182	
Revision A	Floppy Disk Utility User's Guide
JSC-17075	The SMART MIL-STD-1553B Bus Adapter
LEMSCO-16030	Hardware Manual
--	The Master Timing Unit (MTU) Time Bus Interface
--	Adapter (TMIA) User's Guide
--	Master Timing Unit Display/Monitor User's Guide
MIL-STD-1553B	Military Standard 1553B

B.2 HTS DATA MANAGEMENT MICROPROCESSOR EVALUATION

Several advanced microprocessors have capabilities that are needed for avionics system computers. Table B-1 is a survey of 16 and 32 bit microprocessors that are currently available or will be available by late 1982. Since some of the microprocessors are in development, not all performance parameters have been released. The line items in table B-1 were selected as desirable features that should be compared for the HTS microprocessor.

At least two microprocessors should be developed utililzing the DMN MIL-STD-1553B network. It is proposed that a 9445/50 computer be used for early HTS development because the Data Systems Laboratory has sufficient equipment to support an early 1982 start up. A minimum 9445/50 microprocessor will have 128K bytes of RAM, 16 bit word, up to 8 MIL-STD-1553B automatic polling data bus interfaces, MULTIBUS port, NOVALINE computer interface port, 2 RS-232 ports, and hardware floating point arithmetic (available late 1982). This system will have a mapped realtime multitasking operating system and driver software for all user interfaces. A maximum 9445/50 interface would allow

TABLE B-1.- 16 AND 32 BIT MICROPROCESSOR SURVEY

PROCESSOR	9445/50	iAPX 86/10	iAPX 86/20	iAPX 286	iAPX 432	MC68000	NS16032	TMS 99000	Z8003
MANUFACTURER	FAIRCHILD	INTEL	INTEL	INTEL	INTEL	MOTOROLA	NATIONAL	T.I.	ZILOG
AVAILABILITY	1982	STOCK	STOCK	1982	1982	STOCK	1982	1982	1982
DATA BUS INTERNAL (BITS)	16	16	16/64	16	32	32	32	UNKNOWN	16
PHYSICAL ADDRESS SPACE	65 K WORDS	1.0 MBYTES	1.0 MBYTES	16.0 MBYTES	16.0 MBYTES	16.0 MBYTES	16.0 MBYTES	65 K WORDS	8.0 MBYTES
VIRTUAL OR MAP MEMORY	YES	NO	NO	YES	YES	YES	YES	YES	YES
SUPPORT CHIP FAMILY ?	YES	YES	YES	YES	YES	YES	YES	YES	YES
MULTI-PROCESSING?	YES	YES	YES	YES	YES	NO	YES	YES	YES
FORTRAN AND PASCAL AVAIL.	YES	YES	YES	YES	YES	YES	YES	YES	YES
OPTIMIZED FOR ADA ?	NO	NO	NO	UNKNOWN	YES	NO	NO	NO	NO
MIL STD PARTS AVAIL.	YES	YES	NO	NO	NO	NO	NO	NO	YES
SINGLE BOARD µP AVAIL. ?	YES	YES	NO	UNKNOWN	YES	YES	YES	UNKNOWN	YES
POWER	1.5 W @ 5.V	1.4 W @ 5.V	3.7 W @ 5.V	N/A	6.5 W @ 5.V	1.5 W @ 5.V	1.5 W @ 5.V	5. VOLTS	1.6 W @ 5.V
CLOCK FREQ. (MHZ)	24 MHZ,1982 40 MHZ,1934	1.0	5.0	N/A	8.0	10.0	10.0	24.0	10.0
16 BIT INTEGER MULTIPLY	2.9 µSEC	15.1 µSEC	15.1 µSEC	3.0 µ	N/A	7.1 µ	4.6 µ	N/A	7.2 µSEC
32 BIT INTEGER MULTIPLY	14.1 µSEC	75.5 µSEC	19.0 µSEC	15.6 µSEC	6.3 µSEC	34.4 µSEC	7.6 µSEC	N/A	34.3 µSEC
80 BIT IEEE MULTIPLY	N/A	1050.0 µSEC	27.0 µSEC	210 µSEC	25.1 µSEC	N/A	N/A	N/A	N/A
I/O CONTROL INSTRUCTION	0.67 µSEC	1.0 µSEC	1.0 µSEC	N/A	N/A	1.0 µSEC	N/A	N/A	0.9 µSEC

memory to expand to 8 x 10^6 bytes of RAM. All application software would be written in FORTRAN IV through '83 then Ada may be phased in. The user may also select any of the interface port options described in section 3.3. The 9450 is a microprocessor with MIL-STD-1750 instruction architecture.

It is also proposed that a second computer, iAPX432, be developed with the same input/output ports (using 8086 μP as DMT). This system provides the following features not available with the 9445/50.

- Multiprocessing transparent to software
- Transparent post processing
- Very large virtual address space of 2^{40} bytes
- IEEE hardware floating point arithmetic
- 32 bit word
- Redundancy checking
- Ada compatible

The proposed iAPX432 system can be configured with one to six parallel processors with each processor paralleled with an additional processor wired for redundancy checking as shown in figure B-3. A failure of one processor will only cause graceful degradation of the computer system. See figure B-4 for an example block diagram of an HTS iAPX432 multiprocessor system.

Six iAPX432 parallel processors are equivalent to a VAX 11/780 and far exceed the AP101 in number crunching.

An 8086 microprocessor will be used as an interface processor DMT for all data bus protocol. The iAPX432 supports interface processing. This feature will ease the transition from one data bus protocol to another by allowing the protocol overhead to be resident in the 8086 software with no changes required in the application software in the iAPX432.

These two computers will cover a wide range of HTS processing requirements, and the use of only two systems will result in cost savings in software development tools. The proposed VAX 11/780 will provide Ada support for the iAPX432, and the Data Systems Laboratory's NOVA 4X will provide FORTRAN support for the 9445s.

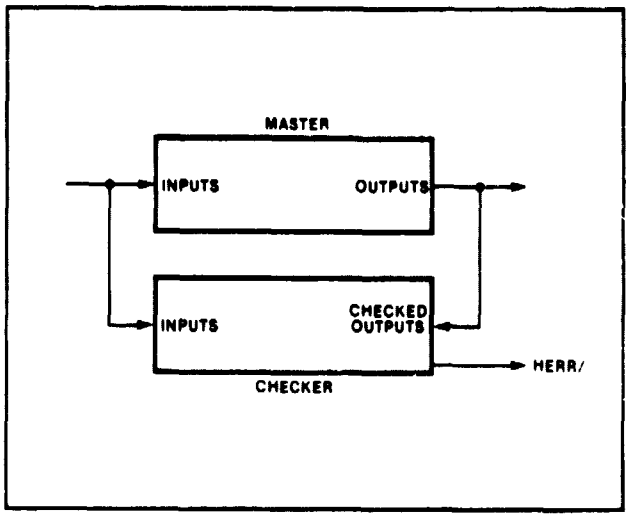


Figure B-3.- Hardware error detection.

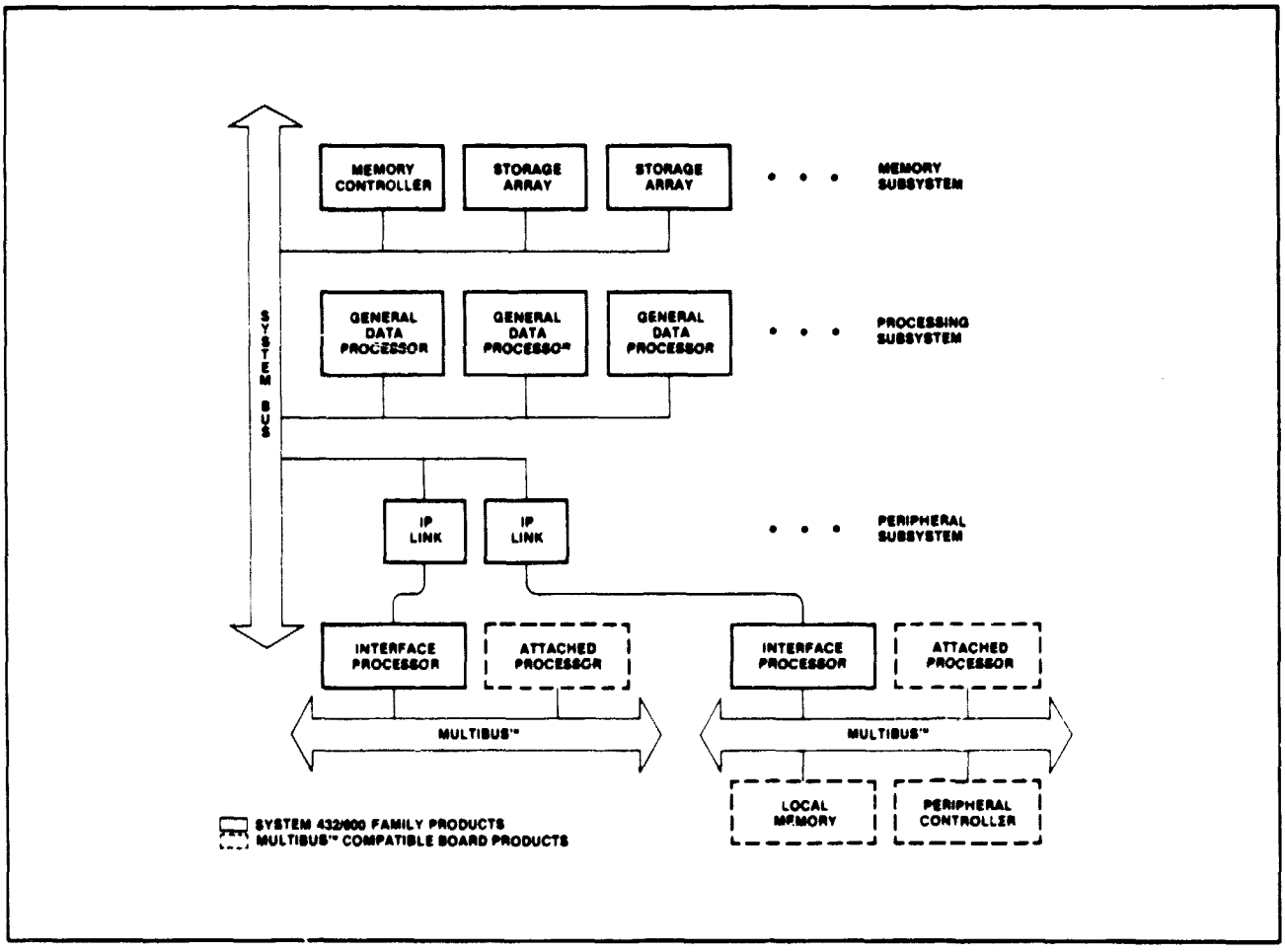


Figure B-4.- System 432/600 block diagram.

The HTS processors may be utilized by the functional areas in several configurations. The first example of a utilization of HTS processor is a Data Management Network terminal shown in figure B-5.

This is an example of a user that has a laboratory with computers and prototype hardware which requires a minimum effort to interface the HTS or ATB. The HTS processor has all hardware/software required by the user to interface the DMN. The user selects the HTS processor or DMT optional subsystem interface that best suits the intended application. A Remote Power Controller (RPC) is available in each DMT to allow the ATB power management subsystem to control primary power to all subsystems.

A second example is a user that utilizes the HTS processor for all of his application software and interfaces his experiment to one of the standard HTS processor interfaces as shown in figure B-6.

This configuration allows a user without computer facilities to develop an ATB application using an HTS processor. As described earlier there are two levels of HTS processors (16 and 32 bit machines) and various configurations with each level. The Data Management software development computer (VAX 11/780) would be used by this user to develop application software in Ada or FORTRAN 77.

The iAPX432/670 is a mid-range member of the integrated 32 bit computer product line. Enclosed in a rack or table top mountable powered and cooled chassis, the System 432/670 includes two General Data Processors (GDP), one Interface Processor, and 512 kbytes of Error Correction Coding (ECC) memory. The System 432/670 includes a 12 slot System Bus backplane that can accommodate subsystem expansion to include two additional GDPs and connections to remote I/O subsystems as well as a total of 1.5 Megabytes of ECC memory. The enclosed MULTIBUS I/O subsystem includes an Intel model SBC 86/12A attached processor with a total of 32 kbytes of EPROM/ROM, 64 kbytes of RAM, and three MULTIBUS backplane slots for user configuration.

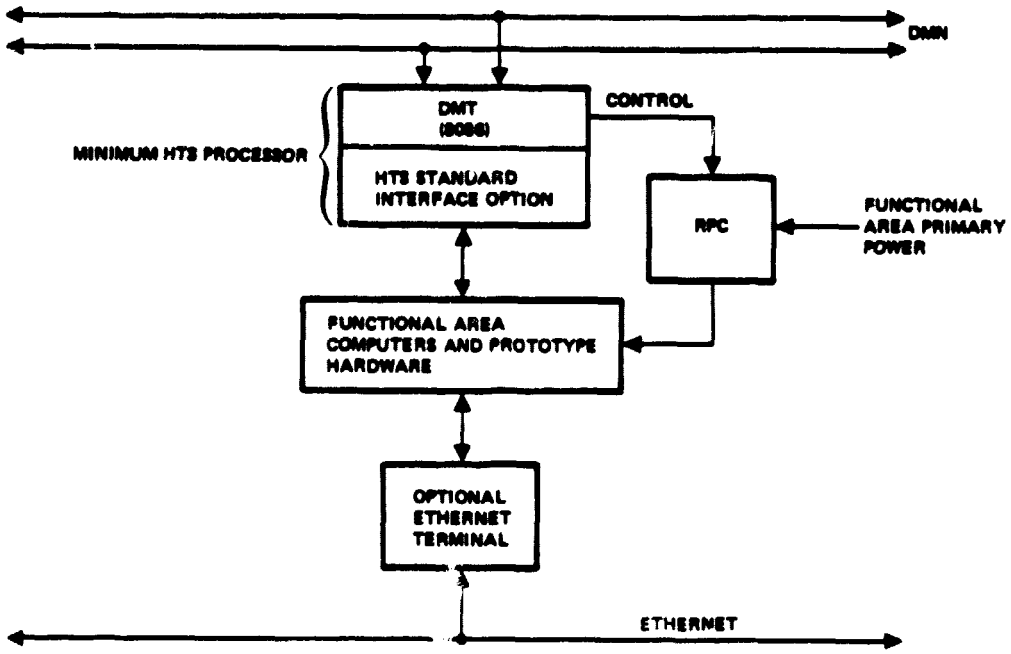


Figure B-5.- Data Management Network terminal.

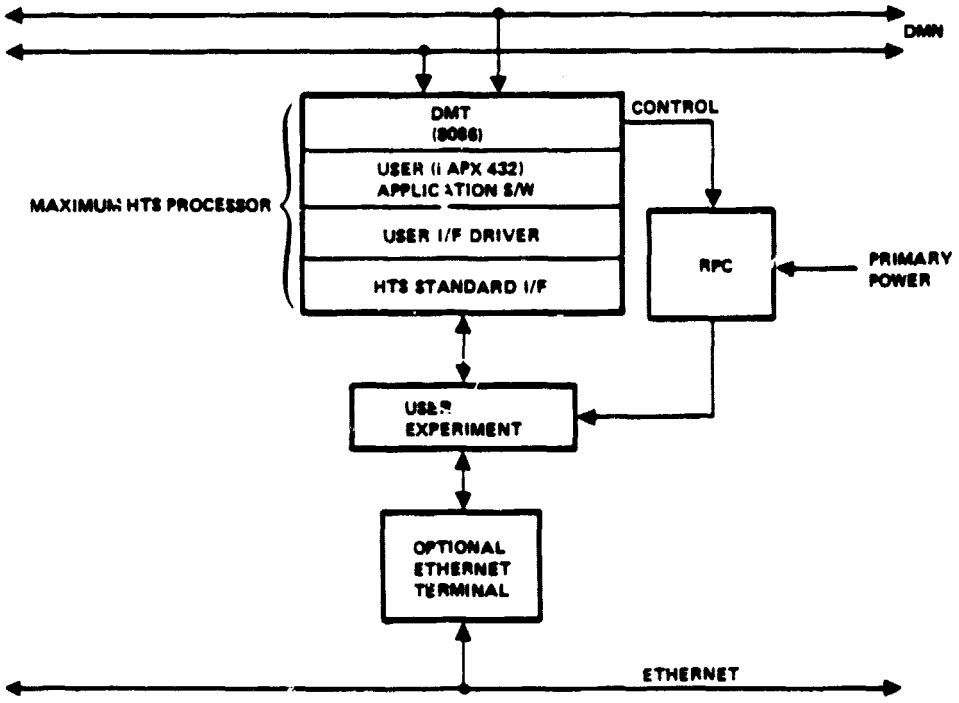


Figure B-6.- Independent HTS processor terminal.

Reference figure B-4 for an example of the advanced architecture of the iAPX432/600 series of computers. This system is in the very early development stage and present prices are quoted for prototyping systems only.

One of the iAPX432 features that apply to avionics systems development is hardware error detection. iAPX432 processors include a facility to support the hardware detection of errors by Functional Redundancy Checking (FRC). At initialization time, each iAPX432 processor is configured to operate as either a master or a checker processor. A master operates in the normal manner. A checker places all output pins that are being checked in the high-impedance state. Thus, those pins which are to be checked on a master and checker are parallel-connected, pin for pin, so the checker can compare its master's output values with its own. Any comparison error causes the checker to assert HERR/(refer to figure B-3.)

B.3 TIMING IN THE HTS

The HTS must furnish a commom clock reference to the distributed processing elements of the system. The time accuracy requirements in the ATB are discussed with respect to relative accuracy between subsystems. It is assumed that the master time source is more accurate than the granularity of the ATB timing cycle.

The master clock rate is 10 kHz. This equates to 1200 master clock pulses per ATB time signal and implies that the timing jitter in the ATB is less than .083 microseconds.

B.4 DEDICATED TIMING BUS

The HTS clock rate is set for an update every 100 microseconds (10 kHz clock). This clock rate establishes the Nyquist limit at 5000 kHz for signal analysis. For perspective, this rate is 400 times faster than that of the space shuttle. The ATB and space shuttle clock rates are compared in figure B-7 where it is assumed the master clock may have a ± .083 microsecond jitter. In the HTS a dedicated time bus is used to transmit one status and three data words at the fixed intervals of 100 microseconds. The one megabit per second MIL-STD-1553B

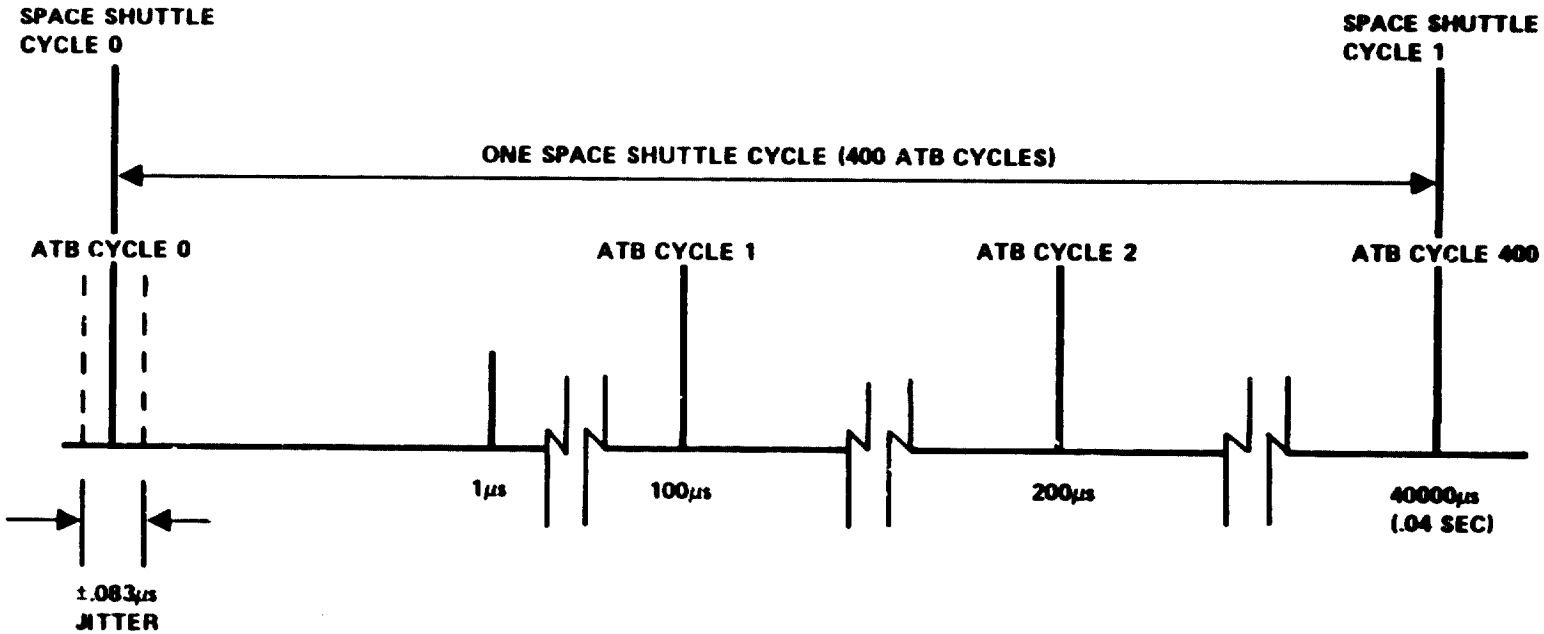


Figure B-7.- ATB vs Shuttle timing.

multiplex data bus will be used for the time bus. At one megabit per second the four words require 80 microseconds for serial transmission. The net 20 micosecond gap is available for the transmitter electronic logic to put the time signal onto the bus.

The MIL-STD-1553B time budget allows approximately 4 microseconds for a round trip signal on the data bus. This restriction sets the maximum length of the bus at approximately 400 meters. A worst case time delay on the bus is less than 2 microseconds.

The receiver electronics requires 5 microseconds for the release of the time data to the individual subsystem. The total transport delay of the time data is as follows:

Transmitter logic	20 µs
Length of data	80 µs
Bus time (worst case)	<2 µs
Receiver case	5 µs
	<107 µs

This delay path is presented in figure B-8.

The bus time differences between subsystems could cause a worst case one cycle asynchronous time tag on subsystem data. The window to cause asynchronous operation is less than 2 microseconds. The worst case is for various subsystems to occasionally be asynchronous by as much as one time gap cycle of 100 microseconds.

Another timing feature is the gap between successive time data words. At the receiver 5 microseconds are used to process the 80 microsecond time data. This allows a read of one buffer while the other buffer is being updated. This arrangement yields a 100 + 15 = 115 microsecond gap for individual buffers.

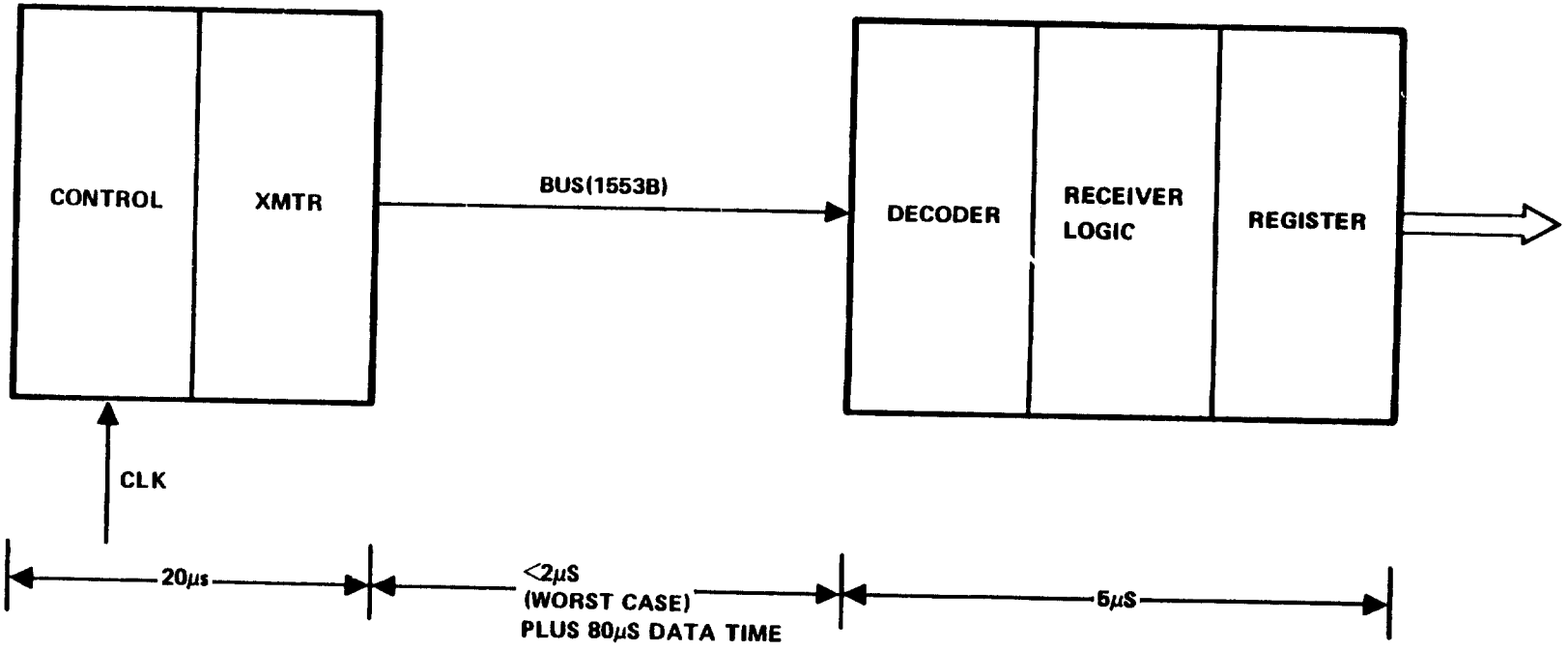


Figure B-8.- Time signal path.

B.5 SYSTEMS MANAGEMENT NETWORK TIMING

The Ethernet protocol will be used for the system management network. The primary characteristics of Ethernet are (reference table B-2):

Data rate: 10 million bits/second

Maximum station separation: 2.5 kilometers

Maximum number of stations: 1024

The worst-case round trip delay is 45 microseconds as presented in the accompanying table. The coaxial cable delay of 13.00 microseconds is included in the total delay. This implies that the worst case one way delay for a signal is 22.5 microseconds.

Ethernet supports variable length data with a set overhead and gap time. The minimum and maximum messages are shown as follows:

Minimum Message	
Overhead	14.4 µs
Message length	36.8 µs
Gap time	9.6 µs
Total	60.8 µs
Maximum Message	
Overhead	14.4 µs
Message length	1200.0 µs
Gap time	9.6 µs
Total	1224.0 µs

The worst case data transmission lag on Ethernet is the 1224 µs process time for the maximum message and 22.5 µs one way network delay for a total 1246.5 µs. Note that short messages have a total lag of approximately 60.8 + 22.5 = 83.3 µs. This value is comparable to the MIL-STD-1553B timing bus delay of 107 µs.

TABLE B-2. - ETHERNET SPECIFICATION: PHYSICAL LAYER

Element	Physical Channel Propagation Delay Budget (Note 1)				
	Unit Steady-State Delay	Unit Startup Delay	# Units Forward Path (Note 2)	# Units Return Path	Total Delay
Encoder	0.1 μS	0	3	3	.60 μS
Transceiver Cable	5.13 nS/M	0	300 M	300 M	3.08 μS
Transceiver (transmit path)	0.50 μS	0.2 μS	3	3	1.50 μS
Transceiver (collision path)	0	0.5 μS	0	3	1.50 μS
Coaxial Cable	4.33 nS/M	0	1500 M	1500 M	13.00 μS
Point-to-Point Link Cable	5.13 nS/M	0	1000 M	1000 M	10.26 μS
Repeater (repeat path)	0.8 μS	0	2	0	1.60 μS
Repeater (collision path)	0.2 μS	0	0	2	0.40 μS
Decoder	0.1 μS	0.8 μS	2	0	1.80 μS
Carrier Sense	0	0.2 μS	3	0	0.60 μS
Collision Detect	0	0.2 μS	0	3	0.60 μS
Signal Rise Time (to 70% in 500 M) (Note 3)	0	0.1 μS	3	0	0.30 μS
Signal Rise Time (50% to 94% in 500 M) (Note 4)	0	2.7 μS	0	3	8.10 μS
		Total Worst-Case Round-Trip Delay			44.99 μS

Note 1: All quantities given are worst-case (both number of units and unit delays per unit).

Note 2: The propagation delay has been separated into "forward-path" and "return path" delay. This is because in one direction it is carrier sense which is being propagated through the channel, and in the return direction it is collision detect which is being propagated. The two signals have different propagation delays.

Note 3: In the worst-case, the propagated signal must reach 70% of its final value to be detected as valid carrier at the end of 500 meters of coaxial cable. This rise time must be included in the propagation delay budget.

Note 4: In the worst-case the propagated collision on the return path must reach 94% of its final value to be detected as a collision at the end of 500 meters of coaxial cable.

The maximum transport lag and asynchronous time tags for the ATB are summarized as follows:

Maximum Transport Lag	< 107 μs
Maximum Asynchronous Time Difference	100 μs

B.6 COMMUNICATION NETWORK OVERVIEW

For ATB network comparison, table B-3 has been prepared. This analysis is concerned with the maximum data exchange rates for each network. All message exchange rates are calculated in bytes/sec for data exchanged. All message exchanges are calculated with a bus commander initiating a message transmit transaction. A message transaction includes all of the following that apply.

- Sync word, sync pulses, etc.
- Command message
- Handshaking
- Word gap
- Message gap
- Hardware handshaking delays
- Fill buffer data
- Message check words or bits
- Message response words of status response
- Identifier
- Data Message

The Maximum Message Rate (MTT) is the worst case condition including all of the above that apply for the completion of a message transaction.

TABLE B-3.- NETWORK MESSAGE EXCHANGE RATES

BUS NAME	BT µs	TYPE P OR S	MINIMUM MESSAGE LENGTH	MINIMUM MESSAGE RATE	MAXIMUM MESSAGE RATE (BYTE/Sec)
ORBITER GPC BUS	1.0	S	2	29.4K	60.6K
MIL-STD-1553B	1.0	S	2	22.7K	90.3K
IEEE-488 (TALKER) HIGH PERFORMANCE	.125	P	2	333K	941K
IEEE-488 (TALKER) STANDARD	.5	P	2	83.3K	235K
ETHERNET	.100	S	46	33.3K	1226K
LCN	.02	P	NA	NA	5M
MULTIBUS	.013	P	2	10M	10M

P - Parallel

S - Serial

APPENDIX C

ALTERNATIVE HTS SYSTEM COMPONENTS

APPENDIX C

ALTERNATIVE HTS SYSTEM COMPONENTS

This appendix provides alternate HTS configurations with pros and cons to the alternative approach.

C.1 ALTERNATIVE HTS DMT

Section B.2 proposed the 9445 microprocessor (a NOVA 4 emulator) or 9450 (MIL-STD-1750) as the minimum configuration HTS computer. The minimum configuration is the Data Management Terminal. As stated, the main reason the 9445 microprocessor was selected is because it emulates the NOVA 4 computer. This feature allows the NASA Data Systems Laboratory NOVA 4X computer system to be an early software development system. The 9445 microprocessor was developed by Fairchild Semiconductor and was released the third quarter of 1981. The support chips such as I/O ports, FPU, memory mapping unit, and DMA controller will not be available until early 1982. The board level system that is now available uses LSI circuits to provide these features. Fairchild Semiconductor and Data General Corp. (manufacturer of NOVA 4) are also involved in a lawsuit on the software license agreements on both the operating system and FORTRAN compiler. A desirable alternate DMT processor is the Intel 8086. This processor is proposed as an I/O preprocessor for the maximum configuration iAPX432 microprocessor. If the 8086 were used as the DMT then a second 8086 development effort could be avoided on the iAPX432. The 8086 is compatible with iAPX432, in fact, the proposed iAPX432/670 systems uses the 8086 as its I/O processor. If the 8086 is selected for the DMT processor, it would require an early procurement of the Intel Intellec system for software development. The software for the 8086 is superior to the 9445 for DMT applications. Ada and Jovial languages are planned for the 8086 in FY82.

It should be noted that the Intellec software development system is required later for the iAPX432. The Intellec provides software development for 17 different Intel microprocessors.

- Hardware and software is available to slave the Intellec development system to a VAX allowing the Intellec to utilize the VAX subsystems.

- A mature system that is in general use throughout the realtime systems community.
- Many vendors are available for second source of components.
- It has mature multiprocessing hardware/software.

C.2 ALTERNATE HTS COMPUTER

The VAX 11/780 is proposed as the HTS computer. Various reasons for its selection are explained throughout this document. The following is a list of the major reasons for selection of the VAX 11/780.

- First mainframe targeted for a certified Ada compiler
- First mainframe to have hardware and software for Ethernet
- Has hardware and software to interface CDC's LCN.
- Software development systems are available for practically all microprocessors.

Alternate computer systems that could be considered are the SEL 32/87 and the Data General MV8000. Since neither of these systems have a price advantage, they are not considered too seriously unless a unique feature can be determined. At this time neither are targeted for Ada, Ethernet, or LCN. Also, neither offer computation speed or software advantages.

C.3 ALTERNATE HTS SYSTEM MANAGEMENT NETWORK

An alternate HTS System Management Network is IEEE-802. IEEE-802 will probably attain formal status by the end of 1982, a little behind Ethernet. The two networks are similar as shown in table C-1.

IEEE-802 promises a slight advantage in data rate. Both systems have carrier-sense, multiaccess with collision detection (CSMA-CD). This feature avoids some of the problems that have been the downfall of similar network protocols.

TABLE C-1.- ETHERNET VS IEEE-802

Feature	Ethernet	IEEE-802
Data rate (Mbits/s)	10	1-20
Max. nodes	1024	--
Max. nodes per segment	100	100
Max repeaters per segment	2	2
Max station separation	2.5 km	2.5 km
Max segment length	500 m	500 m
Medium	Shielded coax, baseband signal	Shielded coax baseband or broadband
Encoding	Manchester phase	Diff. Manchester phase
Topology	Nonrooted tree	Nonrooted tree
Access	CSMA-CD	CSMA-CD or token passing
Levels	1 and 2	1 and 2
	Frame organization	
Synchronization (bits)	64	64
Address (bits)	47	6 to 42
Type or control field (bits)	16 (T)	8 (C)
Data (bytes)	46-1500	46-1500
Frame check (bits)	32	32
Frame spacing	9.6 μs	Depends on data rate